Development and Experimental Verification of a Two-Dimensional Numerical Model of Piezoelectrically Induced Threshold Voltage Shifts in GaAs MESFETs

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Abstract

The results of a combined experimental and analytical investigation of the effects of mechanical stress on DC electrical parameters, particularly threshold voltage, in MESFETs are reported. The theoretical aspect of this study involves a two-dimensional finite element simulation of the same device structure on which measurements were made. In contrast with an approximate analytical calculation reported in the literature in which the stress concentrations which occur at the gate edges were represented by concentrated line forces acting in the plane of the substrate surface, the substrate stresses and resultant piezoelectric charge distributions calculated in this study take into account the two-dimensional nature of the geometry of the gate. Accounting for the two-dimensional nature of the overlayer yields piezoelectric charge distributions that differ from those predicted using the more approximate concentrated force model. The experimental portion of this study involves measurement of DC parameters of devices during the application of external mechanical loads. These loads are intended to simulate mechanical stresses which arise during device processing. By introducing this stress without any additional thermal processing, the impact of residual stresses via the piezoelectric effect on parameters such as threshold voltage can be examined separately from other effects, such as stress enhanced diffusion. It is found that the piezoelectric effect can account for most of the anomalous shift in threshold voltage observed in real GaAs devices.

I Background

It has been known since the early 1980's that GaAs MESFETs exhibit short channel effects that depend on the orientation of the gate with respect to the substrate. It appears that the earliest work carried out in this area is that of Lee *et al* [1], who investigated the dependence of the electrical characteristics of MESFETs on their orientation. The devices were fabricated on (100) surfaces of semi-insulating GaAs substrates. In this study a CVD Si_3N_4 annealing cap was used. Devices oriented in the [011] direction (see Fig. 1 for definition of orientations) exhibited a lower threshold voltage V_T and saturation current I_{DS} than those oriented in the [01$\bar{1}$] direction. Furthermore, the value of V_T varied substantially with gate length L_G for orientation in the [01$\bar{1}$] direction, but it was nearly independent of L_G for the [011] direction over the range of gate lengths which were studied.

Similar work was reported in 1983 by Yokoyama *et al* [2], but this time a CVD SiO_2 annealing cap was used. They noted that the threshold voltage shifts were of opposite sign to that reported by Lee *et al* [1] for the [011] and [01$\bar{1}$] orientations. They also noted that the K-value decreased rapidly for short gate length [011] FETs and they observed that this behavior was absent in [01$\bar{1}$] FETs. In 1983 Sadler and Eastman [3] also reported similar work, this time using a capless anneal in an As overpressure at 800C. They noted that the short-channel effect showed little orientation dependence. They suggested that the dielectric overlayer had a role to play in explaining these effects, and they suspected that a stress driven diffusion mechanism was responsible.

In 1984 Chang *et al* [4] reported that the threshold voltages of FETs in the [011] and [01$\bar{1}$] directions had a strong dependence on their radial distance from the center of the wafer, while [001] and [010] orientation FETs exhibited no such dependence and had better device uniformity. To explain this observation they proposed the presence of a piezoelectric effect, which will be discussed in greater detail below. Later, Ohnishi *et al* [5] resolved the problem of the conflicting data of Lee *et al* [1] and Yokoyama *et al* [2] by attributing the difference in sign of the shift in V_T to the differences in the annealing caps used, namely, CVD SiO_2 films on GaAs are in compression, while CVD Si_3N_4 films are in tension. As will be explained later, the opposite signs of these residual stresses account for the differing V_T shifts.

Two mechanisms have been suggested to explain the orientation dependence of the threshold voltage shift. Both mechanisms most likely play some role. Yokoyama *et al* [2]

and Sadler and Eastman [3] proposed that the orientation effect might be due to anisotropic stress-enhanced preferential diffusion of the implanted dopant materials. They suggested that an increased electron donor concentration in the region of the channel under the gate can occur through the lateral straggle of ions implanted in the n^+ regions and through lateral diffusion of ions during post-implant annealing. The stress between the GaAs substrate and an overlying gate may enhance this diffusion in the direction of the gate. This in turn can change the effective gate length and threshold voltage. Asbeck *et al* [6] and Chang *et al* [4] suggested that residual stresses in the devices induce piezoelectric charge densities that add to the dopant charge densities and thus change V_T.

As mentioned above, mechanical stress in the semiconductor appears to be at the root of the orientation dependent effect. This stress can result from several sources, including thermal expansion mismatch between the substrate and thin film overlayers, alloying of the metal contacts, and wafer deformation due to thermal processing. It is particularly important to note that this stress is enhanced near the gate or overlayer edge due to the stress concentration at the geometrical discontinuity there. It has been shown by a number of authors (see for example Booyens *et al* [7]) that the shear and normal stress components induced by this overlayer or gate are concentrated at the overlayer or gate edge (see Figs. 2a-b.) In fact, we note that the stress components have *singularities* at the gate edge according to an idealization in which the corner is sharp and the material is linearly elastic.

A stress *gradient* in the active channel region induces a piezoelectric charge distribution there. This piezoelectric effect, noted by Asbeck *et al* [6] and others, arises from the fact that the GaAs crystal is non-centrosymmetric (see for instance Nye [8].) The induced charge distribution, which will be denoted by ρ_{pz}, adds to the dopant charge density, thus affecting V_T to some degree. Due to the non-centrosymmetry of the GaAs crystal, the piezoelectric charge density ρ_{pz} induced in [011] FETs is of opposite sign to that in the [01$\bar{1}$] FETs for the same state of stress. Thus, the V_T shifts in these cases will have opposite sign. There should be virtually no effect of stress state on the threshold voltage for FETs oriented with their gates along the [100] directions, as will be shown in Sec. III. This was confirmed by Chang *et al* [4] who, in addition, suggested that the nonuniformity of V_T across a wafer could be explained by the piezoelectric effect. They pointed out that the magnitude of ρ_{pz} under the gate is related to both the overlayer thickness and the gate thickness. During the processing stages the thickness of deposited

films, as well as the amount of undercut on the dielectric openings that are produced by plasma etching is often dependent on radial distance from the center of the wafer. Thus, the piezoelectric effect appears to be a likely source of the systematic radial dependence of MESFET characteristics as well. In addition, the piezoelectric effect has been shown by Chen *et al* [9] to contribute to the shift of V_T with temperature.

II Current Study

In the past, several investigations concerned with the influence of mechanical effects on the electrical properties of field effect transistors have been carried out [6,7]. Although various experimental setups and gate configurations have been used in these studies, the underlying theoretical elastic analyses have been similar in nature to that first presented by Kirkby *et al* [10] in the context of elastic birefringence. These investigators have used clever and elegant approaches to reduce problems of great analytical complexity to simpler, approximate problems for which closed form solutions exist. In particular, the interaction between a stressed overlayer of some lateral extent and the GaAs substrate has been modelled by considering the substrate to be acted upon by an opposed pair of tangential concentrated line loads. These line loads were applied on the substrate surface at the points where the edges of the gate or overlayer met the substrate. This approach emphasizes the severe stress concentration which develops at the edges of the gate-substrate interface. If one considers a thin, stressed overlayer of thickness t (see Fig. 2a), then one can show that the interfacial shear stress is concentrated within a region approximately one fourth of the overlayer thickness from the edge. Nearly all of the load is transmitted from the layer to the edge within a distance from the edge equal to twice the overlayer thickness. In fact, the line load model corresponds to the elasticity solution for the limiting case of the overlayer thickness tending to zero. If one is interested in the stress field in a region far from the points of application of these line loads compared to the thickness of the overlayer, then this solution is adequate. However, since the shear load transmitted between a stressed thin film overlayer and the underlying substrate is actually spread over a distance of roughly twice the thickness of the overlayer (that is, the distance over which the interfacial shear stress is non-zero as illustrated in Fig. 2b), the domain of validity of this approximation is the portion of the substrate which is significantly farther than 2t from either edge of the gate. Unfortunately, the primary region of interest for the problem of threshold shifts in MESFETs is the area immediately under the gate, a region which does not fall within the domain of validity for the line load approximation for typical

overlayer thicknesses. Consequently, use of the line load approximation for the calculation of piezoelectric charges and resultant threshold shifts is unjustified for typical micron and submicron dimensioned MESFETs. In this study, we have attempted to improve on the line load approximation by using a two dimensional finite element method to model more realistically the mechanical interaction between the GaAs substrate and the gate. The results of the mechanical analysis were used to determine the induced piezoelectric charge densities, which in turn were used to estimate the stress-induced threshold voltage shift.

In addition to the two-dimensional numerical simulations, an experimental study was undertaken in order to provide a comparison with the numerical simulations. In the experimental study, DC electrical parameters of self-aligned refractory gate MESFETs were measured while the transistors were subjected to controlled mechanical stress. In earlier work by Asbeck *et al* [6], Onodera *et al* [11], and Chen *et al* [9] the piezoelectric effect on threshold voltage has been studied using thermally mismatched deposited overlayers. These overlayers experience either compressive or tensile stresses, and by etching off various amounts of these layers, the magnitude of these stresses could be varied. However, these experiments are somewhat ambiguous as the device is altered by the deposition process, and the same device cannot be put into both tension and compression. McNally *et al* [12] and Kanamori *et al* [13] have reported a less ambiguous technique in which external mechanical stresses were directly applied to the GaAs substrate. The stress gradients near the edges of thin film overlayers result from the application of external stresses and are similar to those which result from thermally mismatched overlayers and substrates. This technique provides a good means of artificially representing residual stresses in the devices without subjecting the devices to additional thermal or plasma processing. Further processing might introduce additional uncontrolled variables. By introducing these stresses one can examine the ensuing piezoelectric effect. These anticipated effects include V_T shifts, changes in the transconductance g_m and K-value, changes in the gate I-V characteristics, and changes in the subthreshold current slope.

III Theoretical Analysis and Numerical Simulation

The first step in the simulation is to determine the stress and strain fields using the two-dimensional finite element method. The consequent piezoelectric charge distribution is derived from the stress gradients in a way to be described below. Finally, V_T shifts are estimated by calculating the moment of the piezoelectric charge density under the gate.

This method is similar in spirit to the method used by Asbeck *et al* [6] on the basis of the line load approximation. The ensuing analysis is done within the framework of the small strain theory of elasticity. Two assumptions are made at the outset. Firstly, the gate is sufficiently wide in the direction perpendicular to current flow for the deformation to be essentially two dimensional plane strain, and secondly, the elastic properties of the GaAs crystal are isotropic.

It is useful to be able to model devices for which the gate has some general orientation with respect to the crystallographic directions in the substrate. Consequently, it is necessary to introduce two coordinate systems. The first of the two rectangular coordinate systems (x, y, z) is associated with the two-dimensional mechanical problem which will be solved by the finite element method. This coordinate system is tied to the geometry of the device electrodes. Figure 3 shows how the coordinate system (x, y, z) is associated with the spatial orientation of the gate. The y-axis extends along the gate-substrate interface, the x-axis is perpendicular to the interface and extends into the substrate, and the z-axis is parallel to the "long" edges of the gate, with positive z being directed out of the page. The solution for the stress and deformation strain fields is obtained with respect to this coordinate system. A complication which requires the introduction of a second coordinate system arises from the fact that the piezoelectric properties of the GaAs crystal must be related to the crystallographic axes of the substrate. In order to describe the piezoelectric effect, the stress field calculated in the gate coordinate system (which may have an arbitrary orientation relative to the crystal axes) must be transformed into the crystallographic coordinate system. Next, a piezoelectric polarization field is calculated, and then the polarization field must be transformed back into the gate coordinates in order to relate the piezoelectric effects to the geometry of the device.

The zinc-blende structure of GaAs is depicted in Fig. 4. As shown in the figure, a local coordinate system (x_1, x_2, x_3) is associated with the unit cell. The crystallographic x_1-axis is taken to be coaxial with the gate x-axis (that is, devices that have been fabricated on (100) surfaces are considered) and the unit cell is rotated about this axis through an angle α, which is taken as positive when the rotation is counter-clockwise as viewed from the positive x-axis. The direction into the substrate along the x-axis is assumed to be the [100] direction. For an angle α equal to $\pi/4$ the edges of the gate lie along the [011] direction. Other orientations can be modelled by suitable choices of α.

In what follows it will be necessary to distinguish between components of tensorial quantities referred to bases that coincide with either the gate coordinate axes or crystallographic coordinate axes. To that effect, the symbols $[\boldsymbol{\sigma}]$ and $[\boldsymbol{\sigma}]^*$ correspond to the matrices of components of the second rank stress tensor in the gate and crystallographic coordinates respectively. Likewise, $[\mathbf{P}] = (P_x, P_y, P_z)$ and $[\mathbf{P}]^* = (P_1, P_2, P_3)$ represent the arrays of components of the polarization vector in the gate and crystallographic coordinates respectively.

In general, the polarization vector is a linear functional of the stress tensor and is given in coordinate free notation by

$$\mathbf{P} = \mathbf{D}{:}\boldsymbol{\sigma}, \tag{3.1}$$

where $\mathbf{D}$ is the third rank piezoelectric tensor, and : is the tensor dyadic product. In the case of the zinc-blende structure, all but six of the *material* components of the piezoelectric tensor are zero. These six nonzero components of $\mathbf{D}$ all have the same constant value, referred to here as d. This relation can be written in terms of material components as

$$\begin{pmatrix} P_1 \\ P_2 \\ P_3 \end{pmatrix} = d \begin{pmatrix} \sigma_{23} \\ \sigma_{13} \\ \sigma_{12} \end{pmatrix}, \tag{3.2}$$

where in the case of GaAs the constant d is approximately 2.6×10^{-12} coul/newton. Next, it is necessary to transform the relationship (3.2) to the corresponding relationship in terms of gate coordinates.

In transforming from gate coordinates to crystallographic coordinates, stress transforms as a second rank tensor. This transformation can be written as

$$[\boldsymbol{\sigma}]^* = [\boldsymbol{\beta}][\boldsymbol{\sigma}][\boldsymbol{\beta}]^T, \tag{3.3}$$

where $[\boldsymbol{\beta}]$ is the rotation matrix given by

$$[\boldsymbol{\beta}] = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\alpha & \sin\alpha \\ 0 & -\sin\alpha & \cos\alpha \end{pmatrix}$$

Equation (3.3) gives the stress components in material coordinates in terms of the stress components in gate coordinates. Substituting this information into (3.2) yields

$$\begin{aligned} P_1 &= d[\nu\sigma_{xx} - (1-\nu)\sigma_{yy}]\sin\alpha\cos\alpha, \\ P_2 &= -d\sigma_{xy}\sin\alpha, \\ P_3 &= d\sigma_{xy}\cos\alpha. \end{aligned} \tag{3.4}$$

To obtain expression (3.4) only in terms of in-plane stress components, use was made of the fact that for plane strain elastic deformation the out-of-plane stress σ_{zz} is given by

$$\sigma_{zz} = \nu(\sigma_{xx} + \sigma_{yy}),$$

where ν is Poisson's ratio for the substrate (see for instance Timoshenko [14].) Finally, under the aforementioned change of coordinates, the polarization vector components transform as

$$[\mathbf{P}] = [\beta]^T[\mathbf{P}]^*.$$

Therefore the components of the polarization vector in gate coordinates can be written in terms of gate coordinate stress components as

$$\begin{aligned} P_x &= d[\nu\sigma_{xx} - (1-\nu)\sigma_{yy}]\sin\alpha\cos\alpha, \\ P_y &= -d\sigma_{xy}\sin\alpha\cos\alpha, \\ P_z &= d\sigma_{xy}(\cos^2\alpha - \sin^2\alpha). \end{aligned} \tag{3.5}$$

The volume charge density induced by the piezoelectric effect in the substrate is denoted by ρ_{pz} and is given by

$$\rho_{pz} = -\nabla\cdot\mathbf{P}. \tag{3.6}$$

In light of (3.6), the charge density due to the polarization field (3.5) may be simply written as

$$\rho_{pz} = -d\sin(2\alpha)\frac{\partial}{\partial x}\left[(1+\frac{\nu}{2})\sigma_{xx} - \frac{1}{2}(1-\nu)\sigma_{yy}\right]. \tag{3.7}$$

In deriving (3.7), use was made of the fact that in a state of plane strain the fields do not vary in the out-of-plane direction [14]. In addition, one of the momentum balance equations was invoked to suppress the explicit dependence of ρ_{pz} on the shear stress σ_{xy}. It is noteworthy that in the final expression for the charge density, the information pertaining to the orientation of the edge of the FET gate is contained in a multiplicative trigonometric term. Changing the orientation of the device from the [011] direction to the $[01\bar{1}]$ direction merely reverses the sign of the piezoelectric charge, but does not alter its fundamental character. Also, for devices oriented along the $\langle 001\rangle$ directions, $\alpha = n\pi/2, \quad n = \pm 1, \pm 2$, and therefore ρ_{pz} should be zero. The latter result is consistent with the observations of Chang *et al* [4] mentioned earlier.

In the previous paragraphs an expression for the charge density as a function of the state of stress at any point in the GaAs substrate has been obtained. In order to find the charge density distribution in the vicinity of the gate, it is necessary to know the actual stress field induced in the substrate by thin film overlayers, or as in the case of our experiment, to know the stress field induced by the remote loading of the GaAs substrate. At this time, analytic procedures for obtaining a full field solution to the problem depicted in Fig. 3 (which do not make use of restrictive approximations such as line loads) are not known. Instead, the stress analysis is carried out by means of the finite element method (FEM) [15], and the results of this computation are used, in conjunction with (3.7), to numerically determine the piezoelectric charge density distribution in the substrate. As will be shown, it is found that the stress fields and resultant piezoelectric charge densities obtained from this calculation are significantly different from the results obtained using the line load approximation, both qualitatively and quantitatively.

Figure 5 shows a schematic of the mesh that was used for the finite element analysis, along with the symmetry and boundary conditions. The relative dimensions of the mesh are such that the state of stress around a thin metallic gate bonded to a much larger piezoelectric substrate, subject to remote loading, is closely reproduced. Other states of stress, such as those due to pre-existing mismatch strains between the gate and the substrate (which might be incurred during fabrication of the device) can be analyzed using the same scheme.

For the first part of the analysis standard 4-node isoparametric elastic elements were used. The values of the elastic constants assumed for the GaAs substrate were $E = 8.53 \times 10^{10}$ N/m^2 for Young's modulus and $\nu = 0.31$ for Poisson's ratio. For the tungsten silicide gate the values of the elastic constants were assumed to be $E = 6.21 \times 10^{11}$ N/m^2 and $\nu = 0.3$. The entire mesh consisted of 3503 elements and 3633 nodes, with 3233 of these elements being used to model the substrate. Horizontal displacements were prescribed on the leftmost boundary (see Fig. 5) which gave rise to a uniform y-strain in regions of the substrate remote from the gate. The quantity

$$f = d\sin(2\alpha)\left[\frac{1}{2}(1-\nu)\sigma_{yy} - (1+\frac{\nu}{2})\sigma_{xx}\right], \tag{3.8}$$

was computed at the quadrature points of each element that comprised the piezolelectric substrate, and stored for later use in the computation of the charge density distribution in the GaAs crystal.

For the second part of the finite element analysis a least squares smoothing procedure was used to compute the charge density ρ_{pz} from the quantity $f(x,y)$ given in (3.8). The procedure, which is based on a paper by Hinton and Cambell [16], provides a global definition for $f(x,y)$ which is only known at the quadrature points of the elements that comprise the piezoelectric substrate. The smoothing is accomplished by determining the least squares approximation of the function $f(x,y)$ at the nodes of each element. The piezoelectric charge density ρ_{pz} was then computed at the quadrature points by taking the x-derivative of $f(x,y)$ via the standard shape functions. It should be pointed out that the finite element mesh that was used for this part of the computation was the same as that used for the stress analysis, except that the portion which comprises the gate was excluded.

An estimate of threshold voltage shift was made by considering the moment of the piezoelectric charge beneath the midpoint of the gate. The piezoelectric charge distribution was truncated at the bottom edge of the backgate (i.e. substrate channel) depletion layer. Below this, the deep levels in the substrate compensate the piezoelectrically induced charge. The depth of the bottom edge of the backgate depletion layer at $V_G = V_T$ was found by iteratively solving the one-dimensional Poisson equation using the charge density beneath the midpoint of the gate. The differential equation was integrated using the Runge-Kutta-Felhberg method [17] subject to the conditions that the channel is just depleted of carriers and that the Fermi level pinning position in the semi-insulating GaAs bulk is 0.75eV below the conduction band edge. The Si donor profile was taken as

$$N_d(Y) = \frac{D}{R_p} 10^{[0.6146 - 0.7454Y - \exp(0.6371 - 3.378Y)]},$$

where $Y = y/R_p$, $R_p = 3.82 \times 10^{-6}$cm, and $D = 2.7 \times 10^{12}\text{cm}^{-2}$. This profile has been found to provide an excellent fit to measured doping profiles in these devices. The residual acceptor level in the substrate was taken to be 10^{15}cm^{-3}. The piezoelectrically induced charge was included in the space charge profile used to calculate the location of the bottom edge of the backgate depletion layer. This was done because the presence of ρ_{pz} shifts the location of the backgate junction significantly at large stress values. For a given stress level, the threshold shift estimate was obtained by comparing the value of the surface potential from the solution of Poisson's equation including ρ_{pz} to the value of surface potential in the absence of ρ_{pz}. The difference in surface potential is taken as an estimate of the threshold voltage shift induced by the piezoelectric charge.

IV Experimental Setup

Two different setups were used. The first consisted of a steel rod which had been machined flat in the center. The GaAs chip was attached to the bar using Eastman 910 adhesive. A PC board with the center removed was also cemented to the bar (see Fig. 6a). The chips, each containing several devices, were bonded to the PC board. Electrical connections were then made to and from the PC board. The setup was designed to accomodate both tensile and compressive loading. The main uncertainty in this testing method arises from the need to use glue in securing the chip. As long as none of the imposed strain is relieved by deformation of the glue, one can assume that the strain in the GaAs substrate is the same as that in the steel bar.

The second setup eliminated the need for the glue. It consisted of two aluminum blocks (see Fig. 6b), one of which was secured to a base while the other rode on linear bearings to reduce friction. The wafer was placed between two blocks, and the load was applied directly to the wafer by pushing the movable block. The resultant stress was $\sigma = P/wt$, where P is the applied load, w is the width of the chip, and t is the thickness of the chip. The results from the two setups agreed, verifying that deformation of the glue was insignificant.

V Results

The most important result of this study is that the piezoelectric charge distribution predicted using the finite element method is substantially different, both qualitatively and quantitatively, from that predicted using the more approximate line load model. Figure 7 shows a charge density profile as a function of depth into the substrate below the midpoint of the gate. The piezoelectrically induced charge densities predicted by the line load method and by the finite element method are shown for a remote substrate stress of 8.5×10^8 N/m^2. The net donor-acceptor concentration profile is included in the plot for reference. It is clear that the line load model significantly overestimates the amount of piezoelectrically induced charge. This is not surprising since the line load model overemphasizes the shear stress concentrations, resulting in an exaggeration of the predicted shear strain gradients. Note also that the line load model predicts deeper penetration of the piezoelectrically induced charge than the FEM model does. This is particularly important since it is the moment of the charge distribution which determines the threshold shift. The shape of

the piezoelectric charge distributions predicted by the two models can be seen in Figs. 8a-c. These figures show the charge level contours predicted by the FEM model (for both vertical and sloped gate sidewalls) and those predicted by the line load model. In all three figures the remote substrate stress is 8.5×10^8 N/m^2. Throughout the entire region under the gate, the FEM model predicts significantly smaller charge densities than the line load approximation. The contour plots also show that the location of the charge density lobes predicted by the FEM model and line load model are significantly different. The FEM model shows the secondary lobes located closer to the center of the gate, and the primary lobe confined to a region much closer to the surface than the positions predicted by the line load model. Note also that there is little dependence of the overall charge distribution on the gate sidewall slope.

Figure 9 shows that the FEM model predicts substantially smaller threshold voltage shifts that those predicted by the line load model. This result is a consequence of the fact that the FEM model predicts piezoelectrically induced charge which is smaller in magnitude and which has shallower penetration into the substrate than the piezoelectric charge predicted by the line load model. The figure also shows that the threshold voltage shift is not a linear function of the remote substrate stress. There is however a region over which the V_T shift-stress relation is nearly linear.

It is apparent from our computations that any calculation of threshold shift must take into account the doping profile of the specific device which is being modelled. A device in which the bottom edge of the backgate depletion region is shallow will be less sensitive to piezoelectrically induced charge because of a reduction of the total amount of charge which contributes to the threshold shift and due to a reduction of its moment arm. This effect has already been seen in the threshold voltage uniformity improvement observed by Tan *et al* [18] with the addition of a depleted p^+ layer beneath the channel.

A comparison of predicted and measured V_T shifts is shown in Fig. 10. MESFETs having 1μm gate lengths and oriented along perpendicular directions ([011] and [01$\bar{1}$]) were loaded in tension. Their threshold shift was measured as a function of remote substrate stress. As shown in the figure, the sign of the V_T shift changes with orientation. It was also observed that for devices loaded in tension, the sign of the threshold shift is opposite to that of devices loaded in compression. These observations provide very strong evidence of the piezoelectric nature of the effect. Figure 10 shows reasonable agreement between the

predictions of the FEM model and the experimental data. By contrast, the line load model substantially overestimates the V_T shift. These results suggest that accurate modelling of substrate stress fields is essential to accurate prediction of piezoelectric effects.

Although only threshold shifts were modelled analytically in this study, other DC parameters were measured experimentally. Figure 11 shows the percent shift in K-value for a 1.6μm [011] MESFET as a function of stress. The tensile stress induces negative charge under the gate, pushing the channel closer to the gate and thus raising the K-value. Conversely, compressive stress reduces the K-value. The reversal of the effect for oppositely signed stress again points to the piezoelectric nature of the effect.

VI Conclusions

Measurements carried out on GaAs MESFETs under applied loads of both signs and on devices of both [011] and [01$\bar{1}$] orientations unambiguously confirm the existence of a piezoelectrically induced threshold voltage shift. A comparison was made between the approximate line load method of modelling substrate stress fields, previously used by workers in this field, and the finite element method used in this study. The piezoelectric charge densities predicted by the two models were found to be substantially different both qualitatively and quantitavely. This results from the fact that the simplifying assumptions used to construct the line load model are inappropriate for accurately determining stress fields beneath micron and sub-micron dimensioned gates. Good agreement was obtained between measured threshold voltage shifts and those predicted by the finite element method model. These results clearly show the need for accurate modelling of mechanical stresses when attempting to model piezoelectric effects.

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Figure Captions

1. Illustration defining the orientations of the MESFETs.

2a. Idealized geometry of substrate-overlayer interface.

2b. Schematic representation of interfacial shear stress for the case of a stressed overlayer on a substrate.

3. Schematic of the idealized problem in which a metallic gate is bonded to a semi-infinite subtrate. The substrate has been subjected to a remote stress σ.

4. Schematic of the sphalerite structure of GaAs, with crystallographic coordinate axis indicated. A sketch of the substrate shows the orientation of the crystallographic coordinates relative to the edge of the gate.

5. Schematic representation of the finite element mesh used for stress analysis, indicating boundary conditions and relative dimensions.

6a. Illustration of the first experimental setup used to load MESFETs in either tension or compression.

6b. Illustration of the second experimental setup used to load MESFETs in compression.

7. Plot showing charge density as a function of depth below the midpoint of the gate. Negative charge densities have been multiplied by minus one to allow them to be displayed on a logarithmic scale. Values for the line load and FEM solutions were taken along the column of quadrature points closest to the midplane of the gate. The line load solution used to generate this data is taken from Asbeck *et al* [6].

8a. Regularly spaced contours of piezoelectric charge density, obtained from FEM analysis for vertical gate sidewalls. Contour a corresponds to a level of $-2.18 \times 10^{16}\text{cm}^{-3}$, contour g corresponds to a level of $2.18 \times 10^{16}\text{cm}^{-3}$, and intermediate contour levels are obtained by uniform increment of $7.25 \times 10^{15}\text{cm}^{-3}$. The portion of the gate and substrate shown in this diagram extends 0.5μm in the vertical direction and 0.8μm in the horizontal direction.

8b. Regularly spaced contours of piezoelectric charge density, obtained from FEM analysis for sloped gate sidewalls. Contour a corresponds to a level of $-2.18 \times 10^{16}\text{cm}^{-3}$,

contour g corresponds to a level of $2.18 \times 10^{16}\text{cm}^{-3}$, and intermediate contour levels are obtained by uniform increment of $7.25 \times 10^{15}\text{cm}^{-3}$. The portion of the gate and substrate shown in this diagram extends 0.5μm in the vertical direction and 0.8μm in the horizontal direction.

8c. Regularly spaced contours of piezoelectric charge density, obtained from line load analysis. Contour a corresponds to a level of $-1.88 \times 10^{17}\text{cm}^{-3}$, contour g corresponds to a level of $1.88 \times 10^{17}\text{cm}^{-3}$, and intermediate contour levels are obtained by uniform increment of $6.25 \times 10^{16}\text{cm}^{-3}$. The portion of the gate and substrate shown in this diagram extends 0.5μm in the vertical direction and 0.8μm in the horizontal direction.

9. Plot of the relation between the threshold voltage shift and remote substrate stress. The gate length is 1μm. The line load model data cannot be used to predict ΔV_T for [011] FETs in tension when the remote substrate stress exceeds $1.7 \times 10^7\text{N/m}^2$. This is due to the specifications of the devices modeled in this paper.

10. Plot of the relation between the threshold voltage shift and remote substrate stress, including experimental data. The gate length is 1μm.

11. Plot of the relation between the percent shift in K-value and remote substrate stress obtained from experiments. The gate length is 1.6μm.

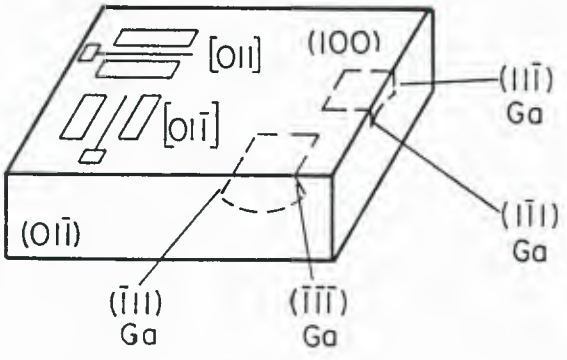

Figure 1

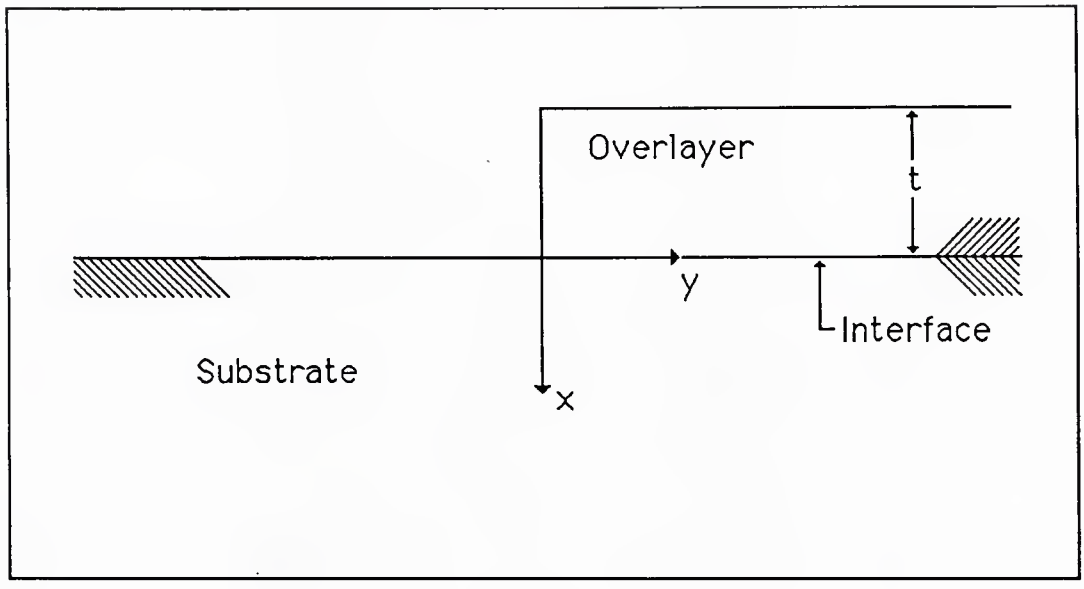

Figure 2a

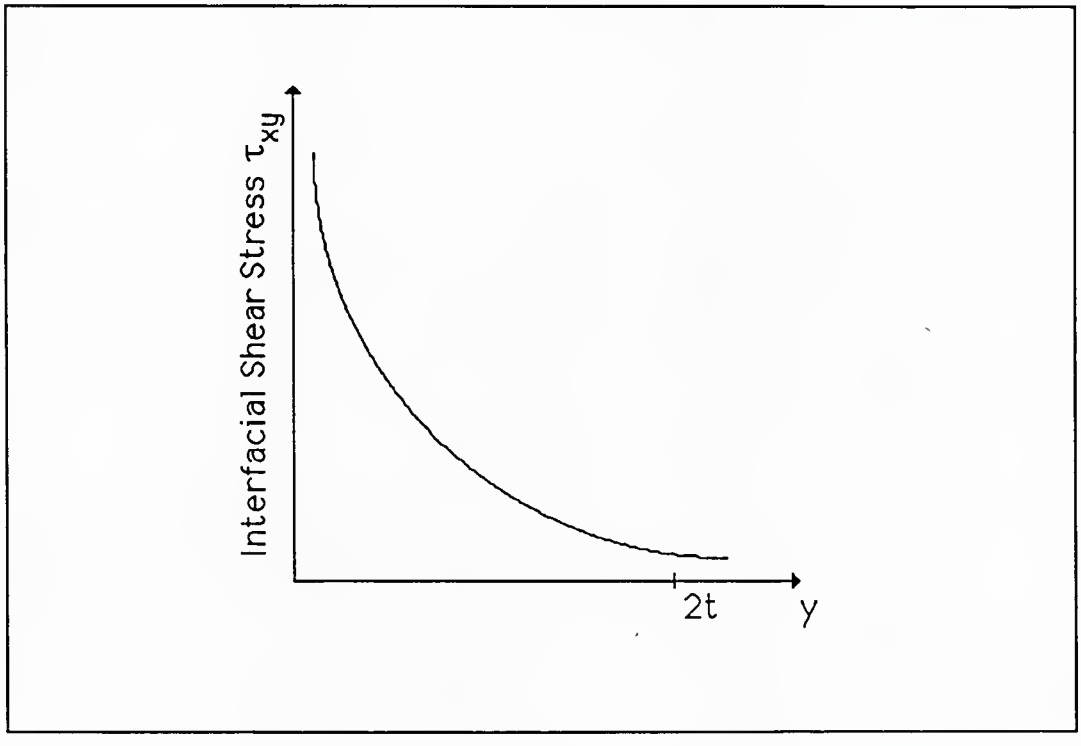

Figure 2b

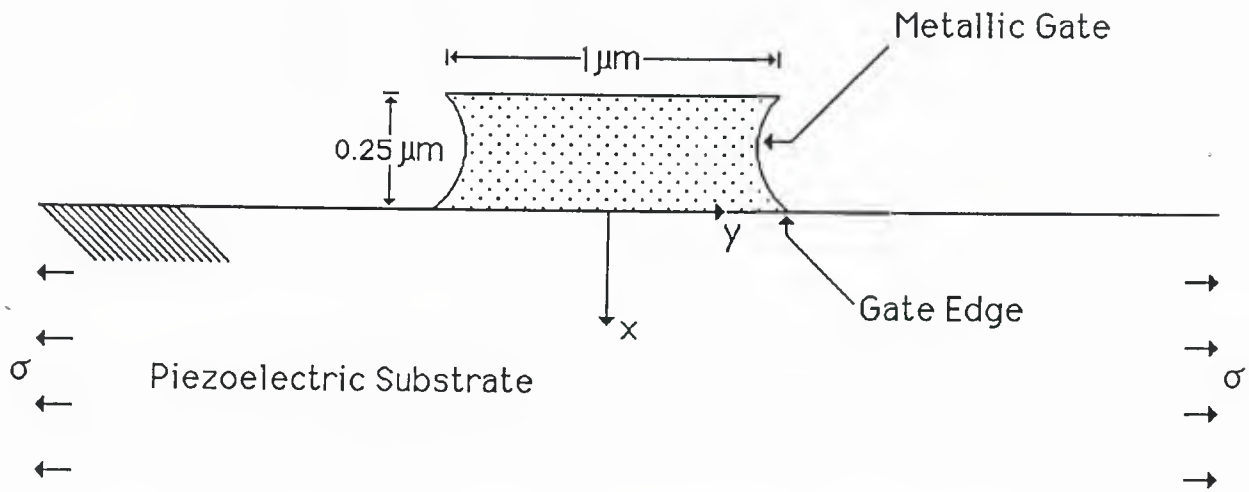
Metallic Gate
1 μm
0.25 μm
y
x
Gate Edge
σ
Piezoelectric Substrate
σ

Figure 3

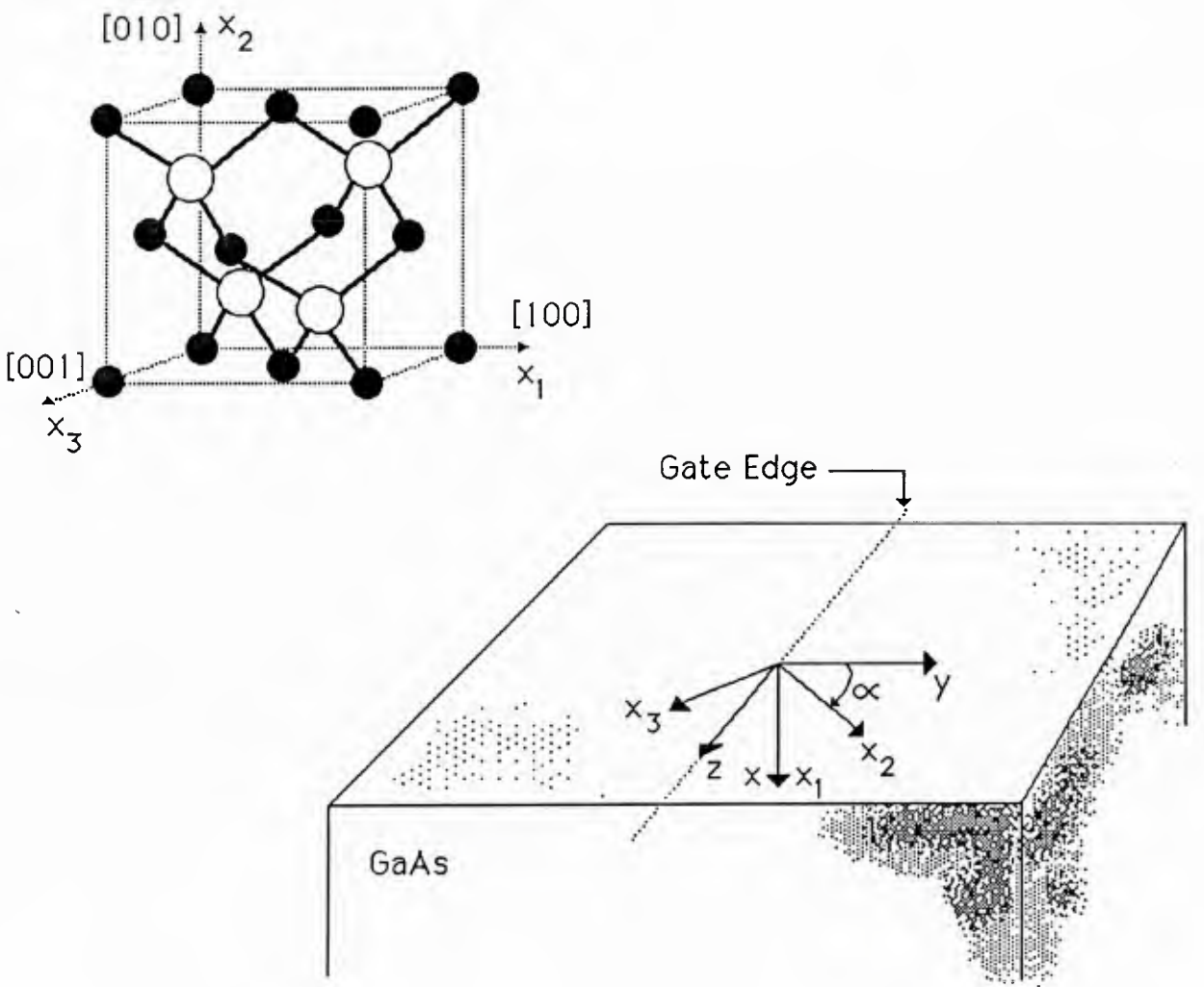

Figure 4

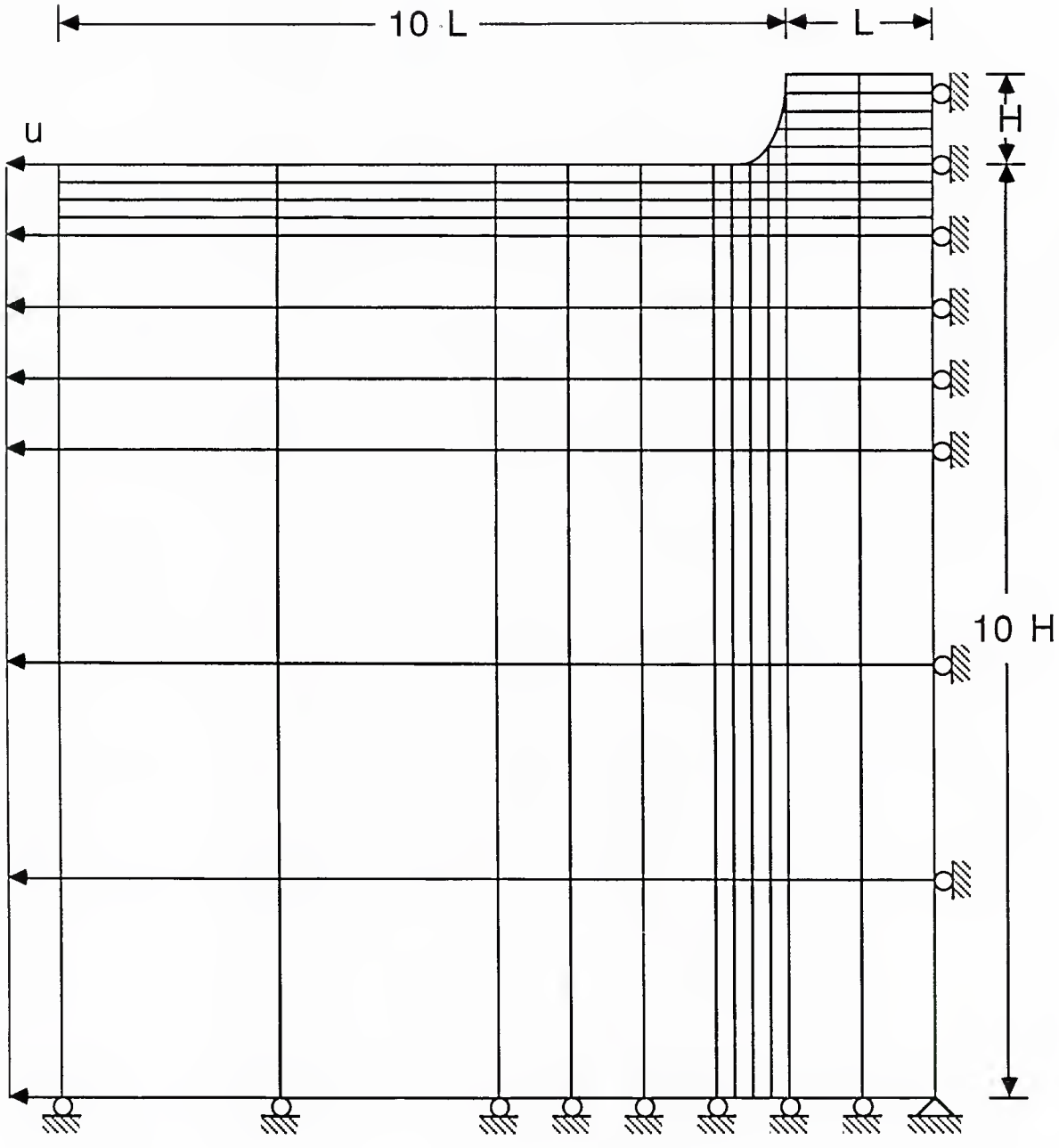

Figure 5

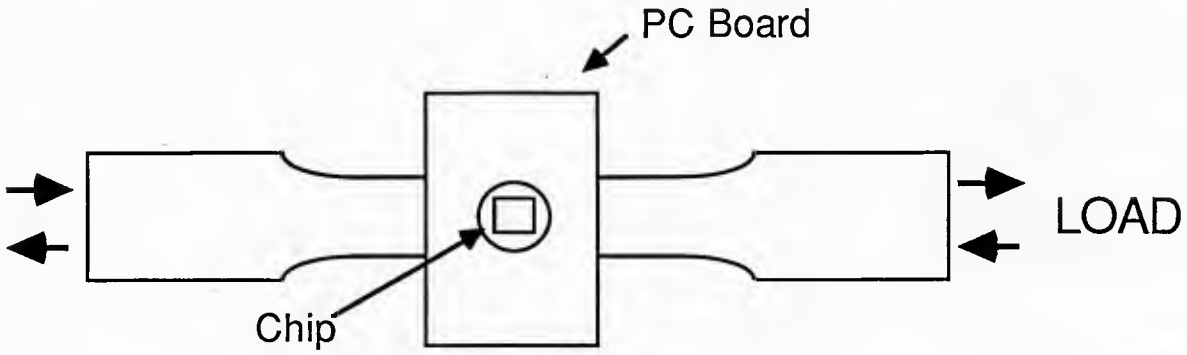

Figure 6a

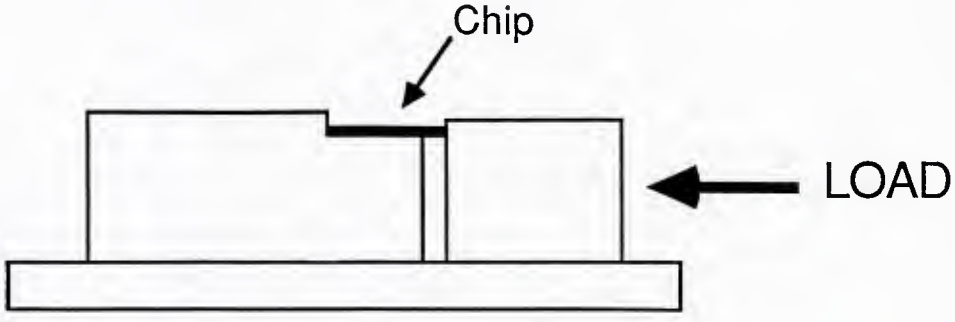

Figure 6b

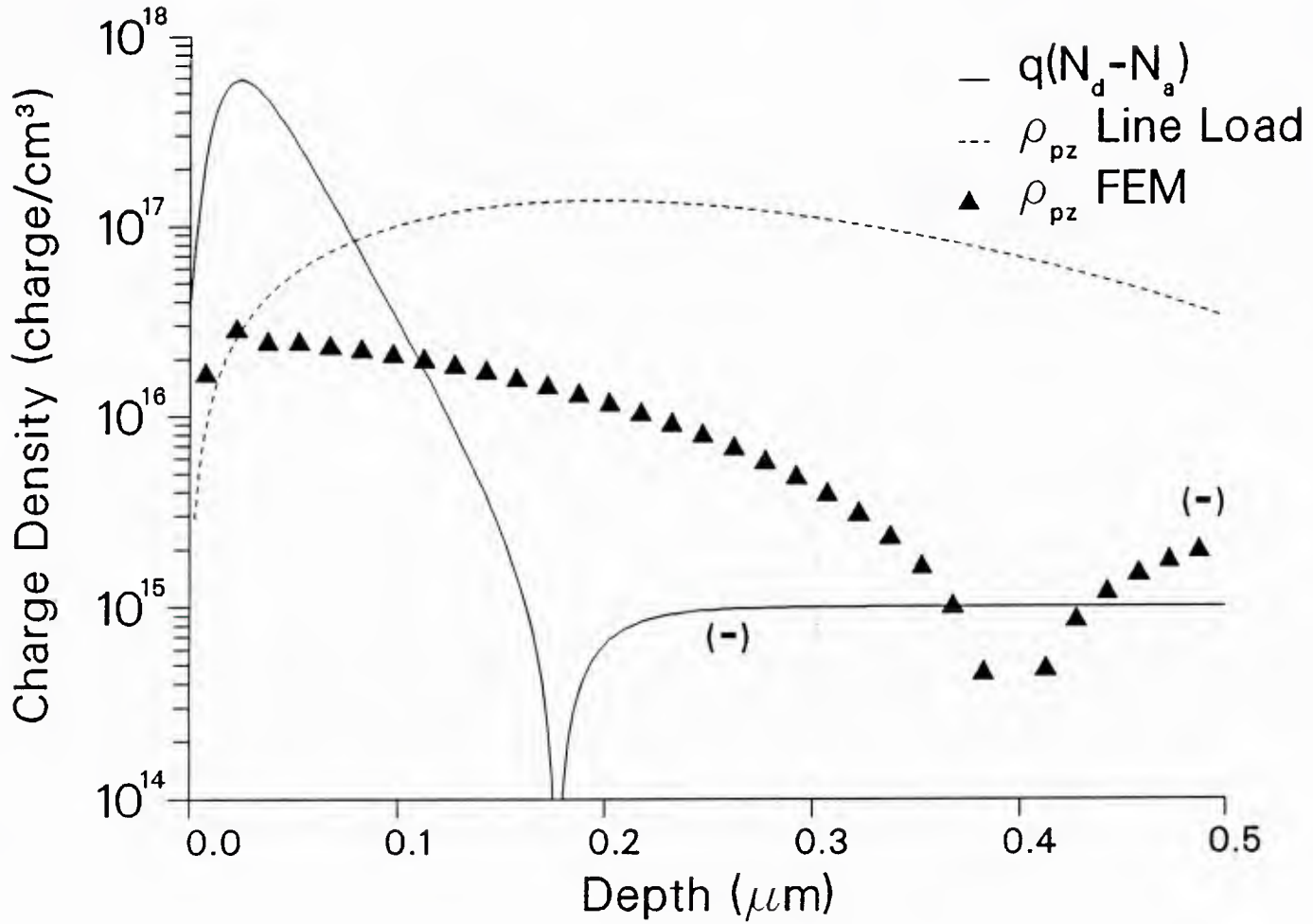
10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
Charge Density (charge/cm^3)
0.0
0.1
0.2
0.3
0.4
0.5
Depth (μm)
q(N$_d$-N$_a$)
ρ_{pz} Line Load
ρ_{pz} FEM
(-)
(-)

Figure 7

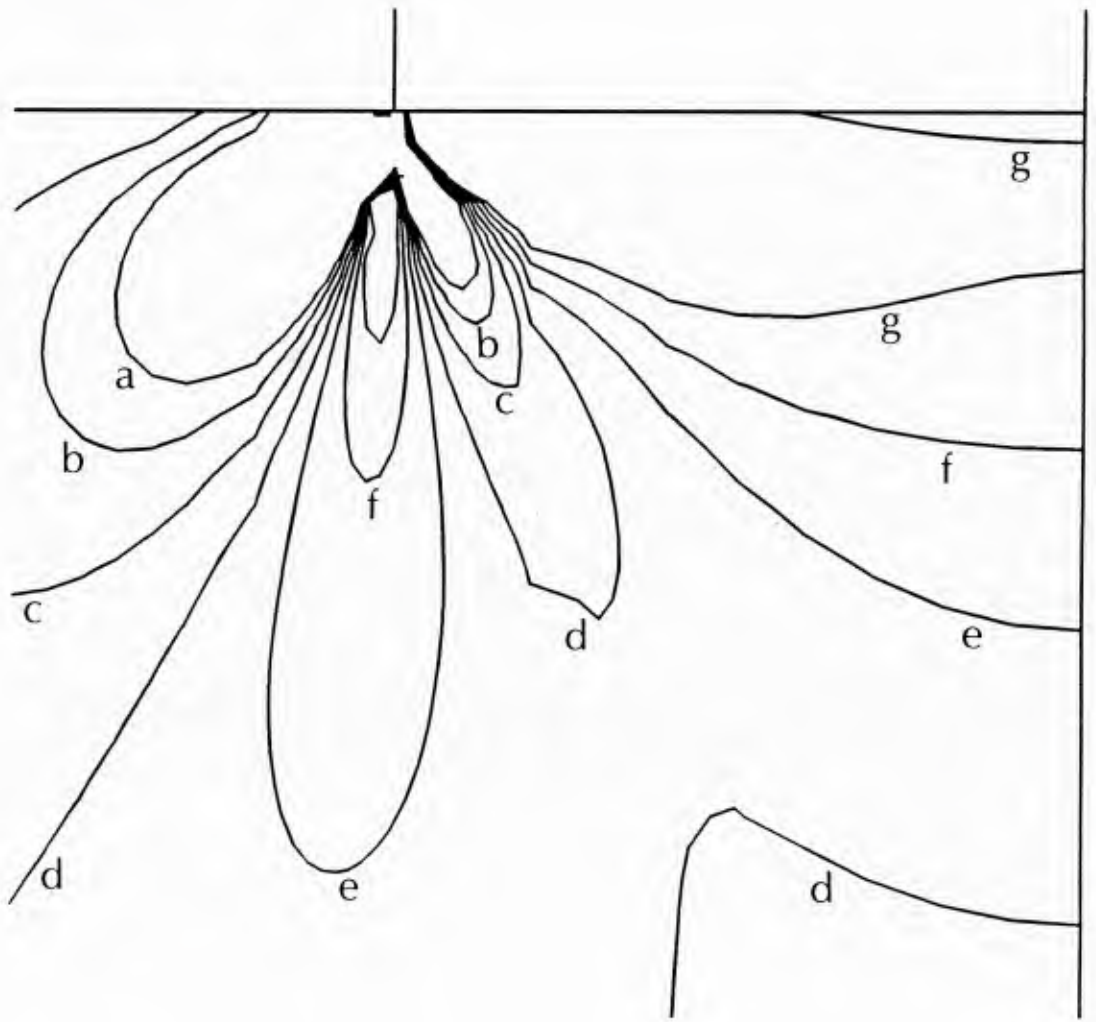

Figure 8a

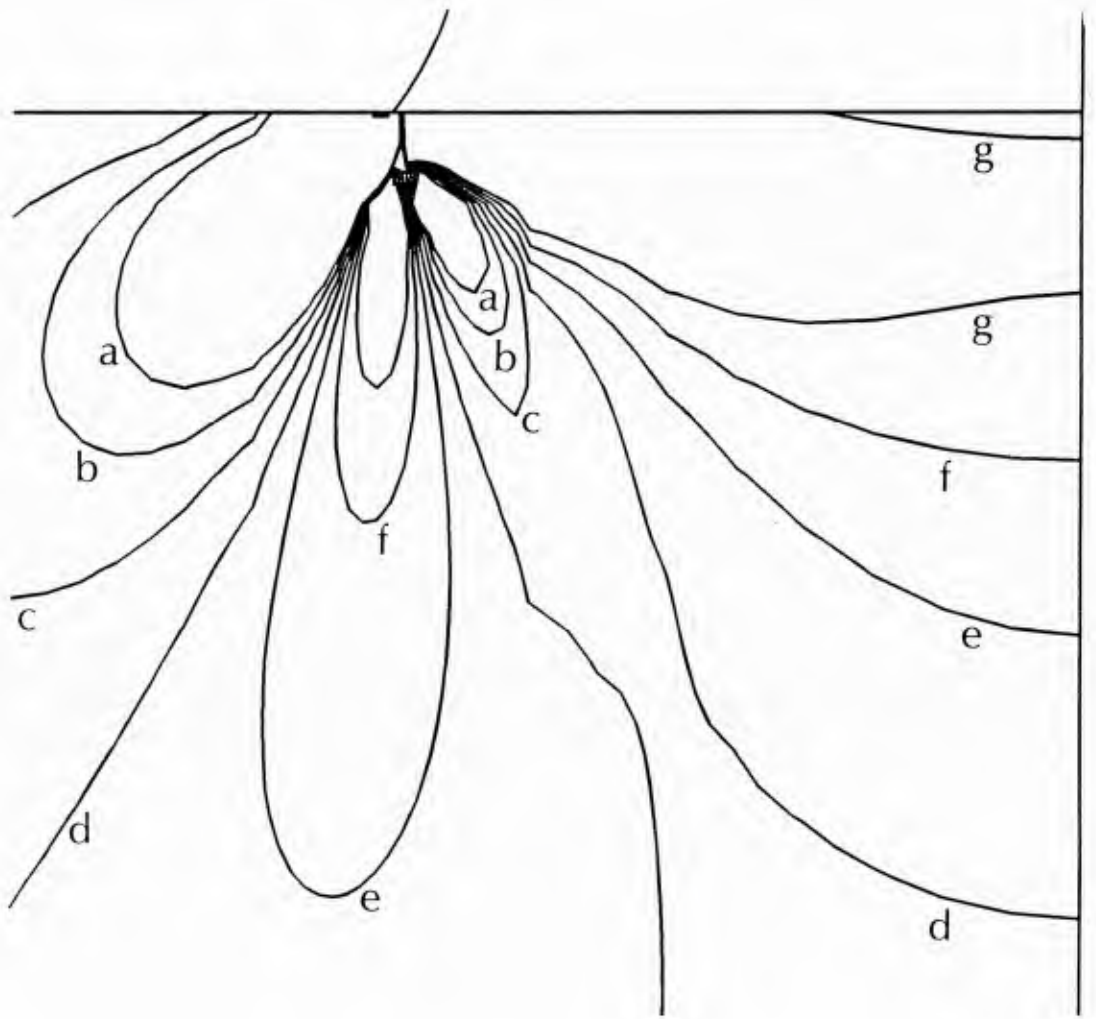

Figure 8b

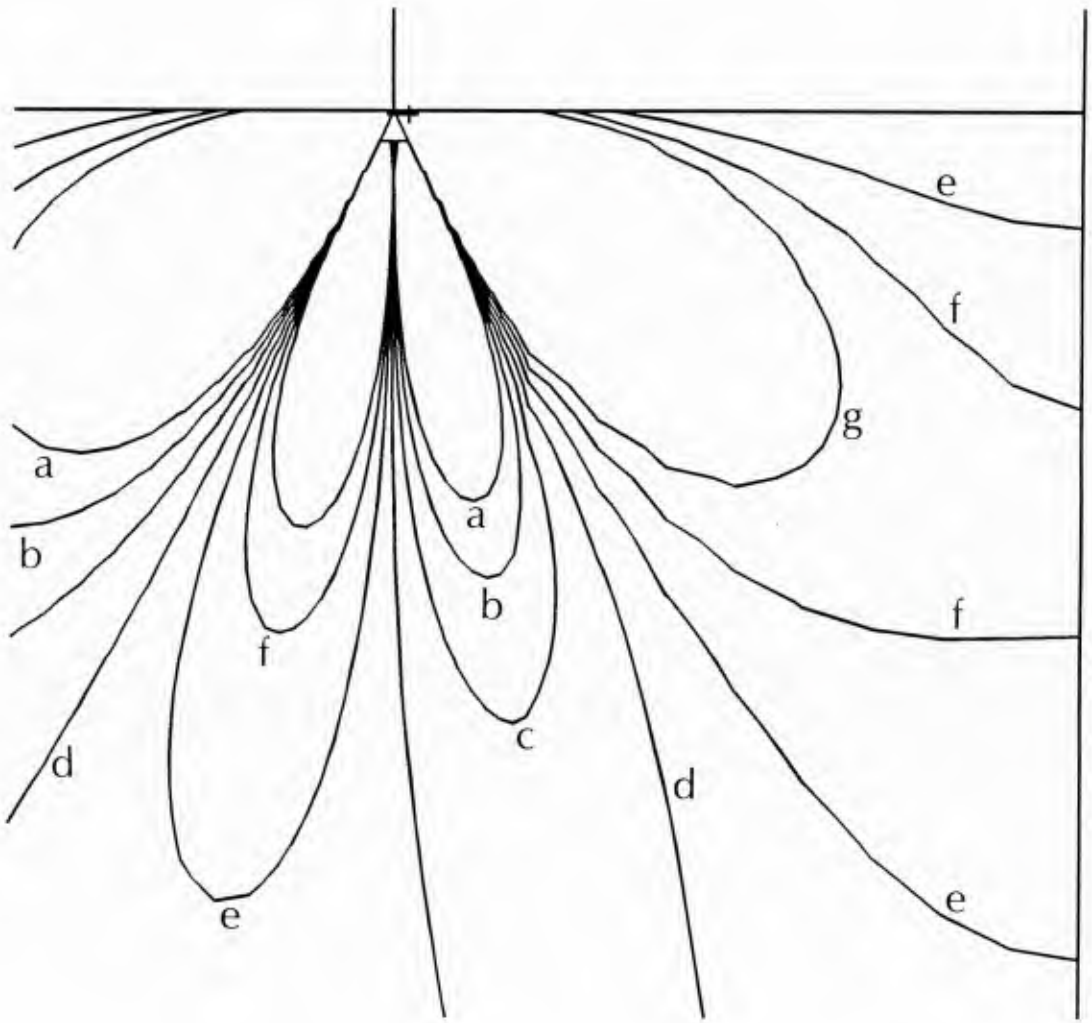

Figure 8c

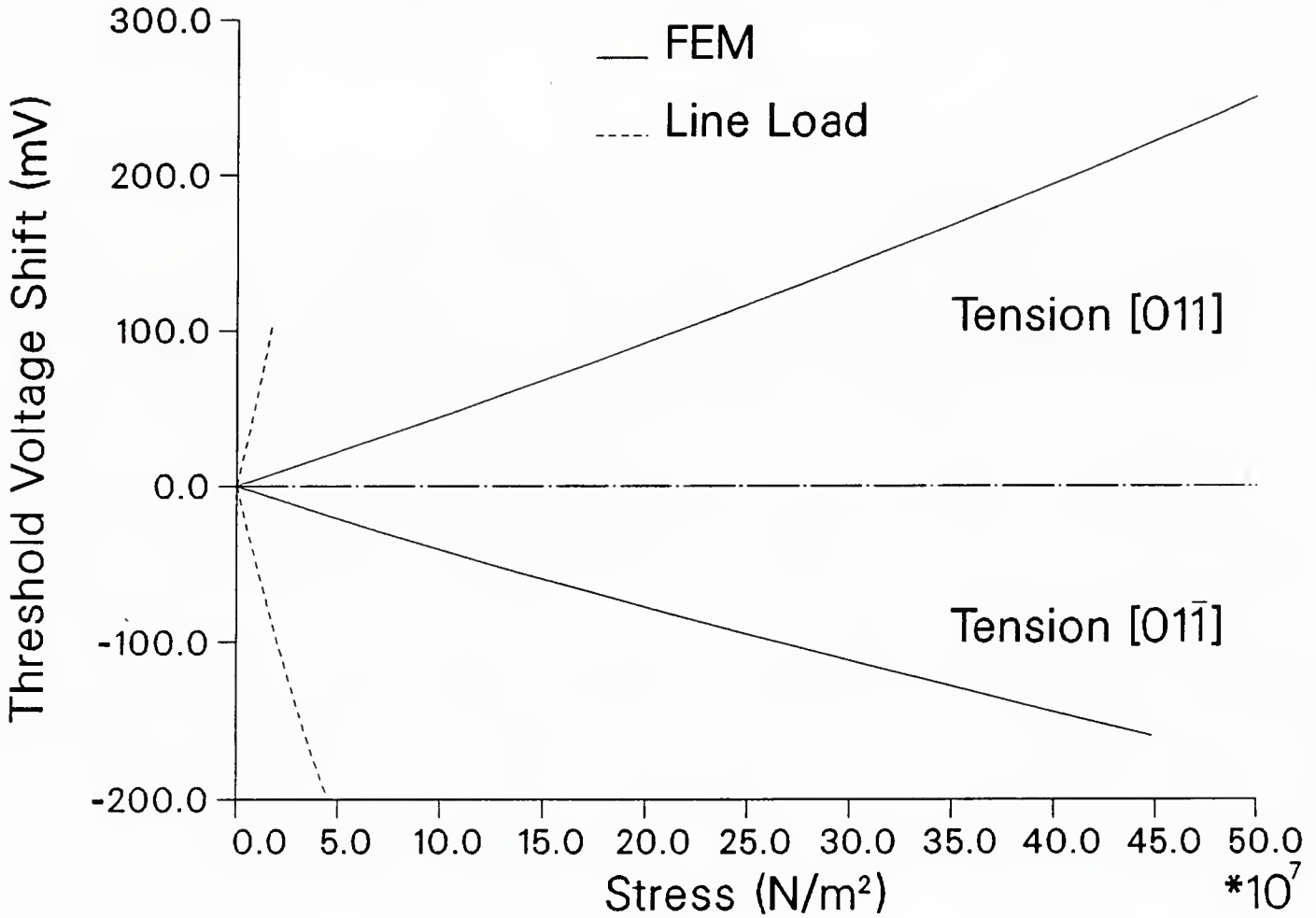
300.0
200.0
100.0
0.0
-100.0
-200.0
Threshold Voltage Shift (mV)
FEM
Line Load
Tension [011]
Tension [01$\bar{1}$]
0.0 5.0 10.0 15.0 20.0 25.0 30.0 35.0 40.0 45.0 50.0
Stress (N/m²)
*10⁷

Figure 9

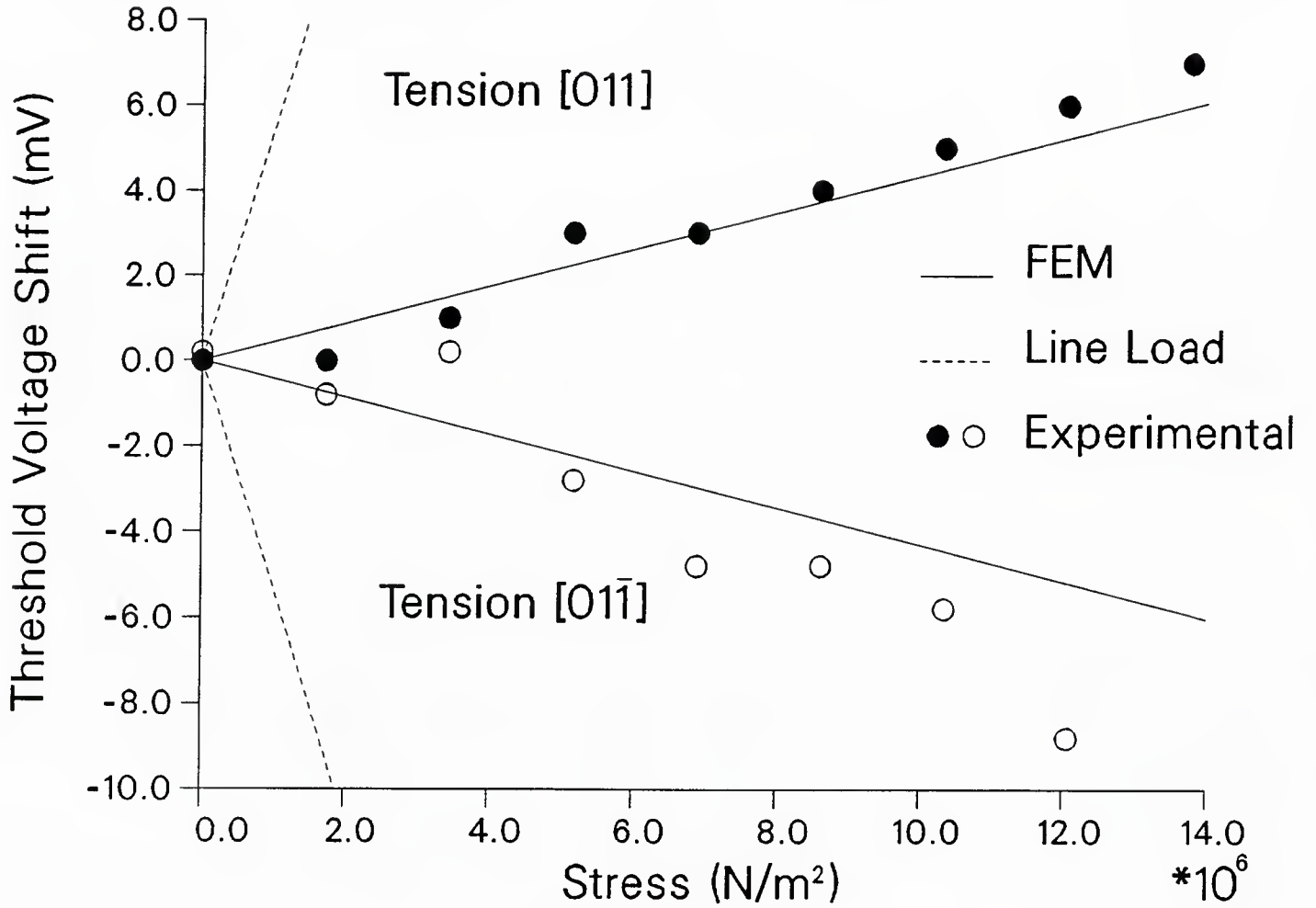
Threshold Voltage Shift (mV)
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
Tension [011]
Tension [01$\bar{1}$]
FEM
Line Load
Experimental
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
Stress (N/m^2)
*10^6

Figure 10

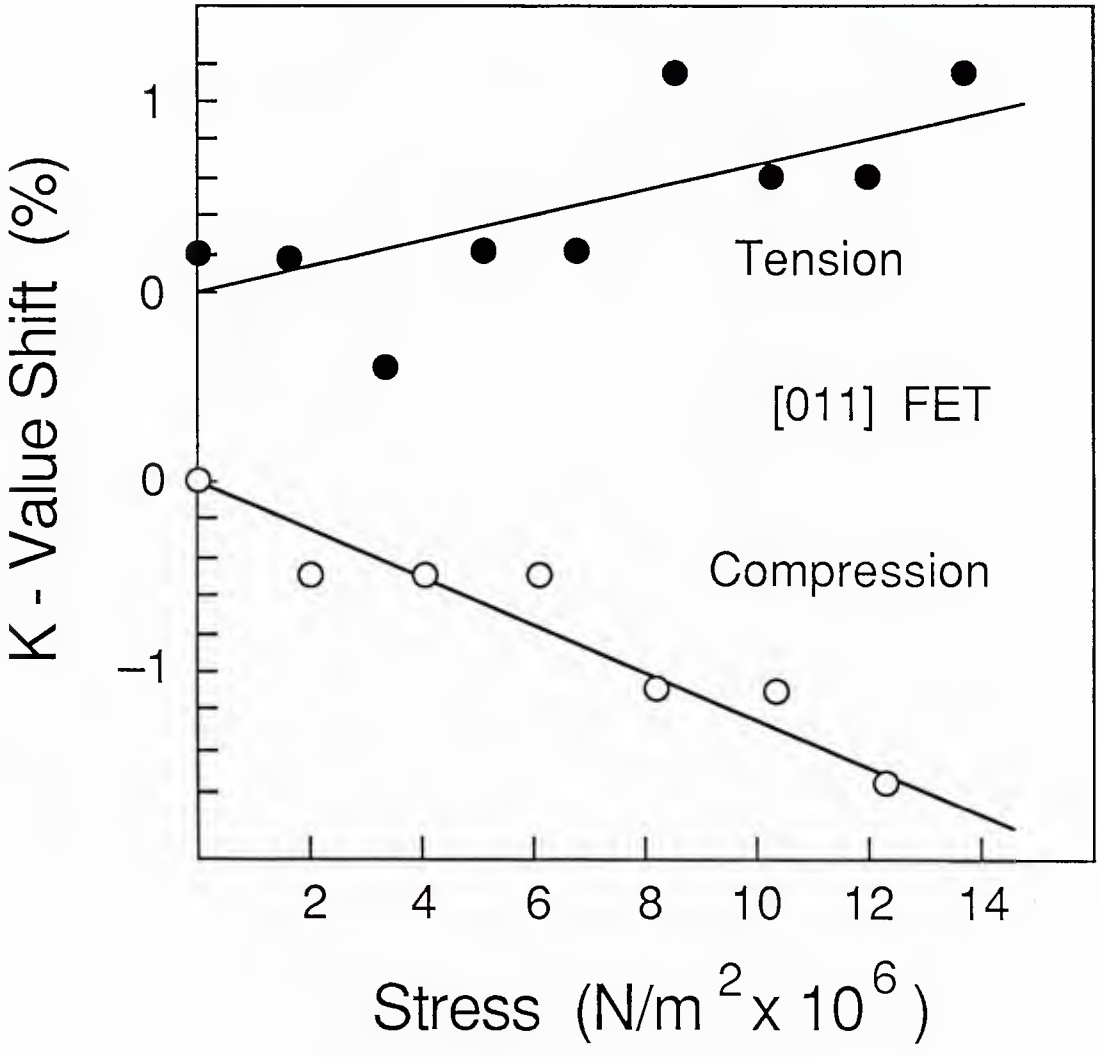
K - Value Shift (%)
1
0
0
−1
Tension
[011] FET
Compression
2
4
6
8
10
12
14
Stress (N/m 2 x 10 6)

Figure 11